A SKIROC2-based prototype electronics system for Silicon PIN array

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**Abstract:**

A prototype electronics system, based on the SKIROC2 Application-Specific Integrated Circuit (ASIC), for silicon PIN (Si-PIN) array has been developed. The system consists of two kinds of electronics modules: the Front-End Board (FEB) module and the Data Interface (DIF) module. The FEB, which carries the SKIROC2 ASIC and the Si-PIN diodes array, is in charge of particle detection and analog to digital signal conversion, and the DIF is designed to control the FEB and to transfer data to PC via a USB bus. The equivalent noise level of all the 64 channels are below 0.4 fC, while most of them are below 0.2 fC. The dynamic range is up to +3000 fC with an Integral Non-Linearity (INL) of 0.2 % and gain uniformity better than 5 %. A kind of Si-PIN diodes named S5980 from HAMAMATSU is coupled with the system to assess its performance. The X-rays test from a radioactive source (241Am) and cosmic rays test have been carried out. The energy resolution with X-rays, at 59 keV, reaches up to 13.3 % (in RMS). The Signal-to-Noise Ratio (SNR) is about 10.9 for Minimum Ionizing Particle (MIP). The details of the system, together with the test results, are presented in this paper.

**Key words：**SKIROC2, Silicon PIN diode, Front-end electronics, Readout system.

# Introduction

Silicon PIN (Si-PIN) diode, which has advantage of high energy resolution and high position resolution when implementing photoelectric conversion, has been widely used in high-energy physics experiments such as the CALorimetric Electron Telescope (CALET) and the International Linear Collider (ILC) prototype1 2. The next generation experiments, such as the Circular Electron Positron Collider (CEPC) 3 and the ILC, demand finer granularity for their detectors to achieve the ability of higher energy resolution and more accurate particle identification. This trend means more readout channels for the Si-PIN diodes, leading to a requirement for a new electronics system with the feature of higher integration and lower power consumption than the tradition ones4.

The Silicon Kalorimeter Integrated ReadOut Chip 2 (SKIROC2)5, which is an ASIC developed in the CALICE collaboration aiming for the Si-PIN signal readout, integrates 64 channels on one chip and has the feature of low noise and large dynamic range. In this paper, a multi-channel electronics system, based on SKIROC2 ASIC, is designed and implemented. It has advantages of low noise level (0.2 fC), high dynamic range (0 to +3000 fC) and high integration (64 channels). A kind of Si-PIN diode named S5980 from HAMAMATSU is coupled with the system to test its performance. The details of the design and tests are presented below.

# Implement of the system

Shown in Fig. 1 is the block diagram of the readout electronics, which is separated into two parts so that it has the potentiality for expansion of more readout channels by only changing the Front-End Board (FEB). The FEB, which carries a Si-PIN diodes array and an ASIC of SKIROC2 on it, can provide high voltage to the Si-PIN and process signals coming from the Si-PIN. The FEB is configured by the Data InterFace board (DIF) connected to it and sends data to the DIF, which then transfers data to PC via USB interface after packing process.



Fig. 1 Block diagram of the electronics system, which mainly consists of the FEB and the DIF.

## ASIC

The core of the FEB is the SKIROC2 ASIC. Fig. 2 presents the schematic illustration of one channel of SKIROC2, on which 64 same channels are integrated. Each channel is composed of a Charge-Sensitive Amplifier (CSA), two slow shapers with different gains, one fast shaper with a discriminator, a time-to-digital convertor (TDC) for time measurement, three Switched Capacitor Arrays (SCA) of 15 depth to store analog signal and an Analog-to-Digital (ADC) to convert signal from analog to digital.

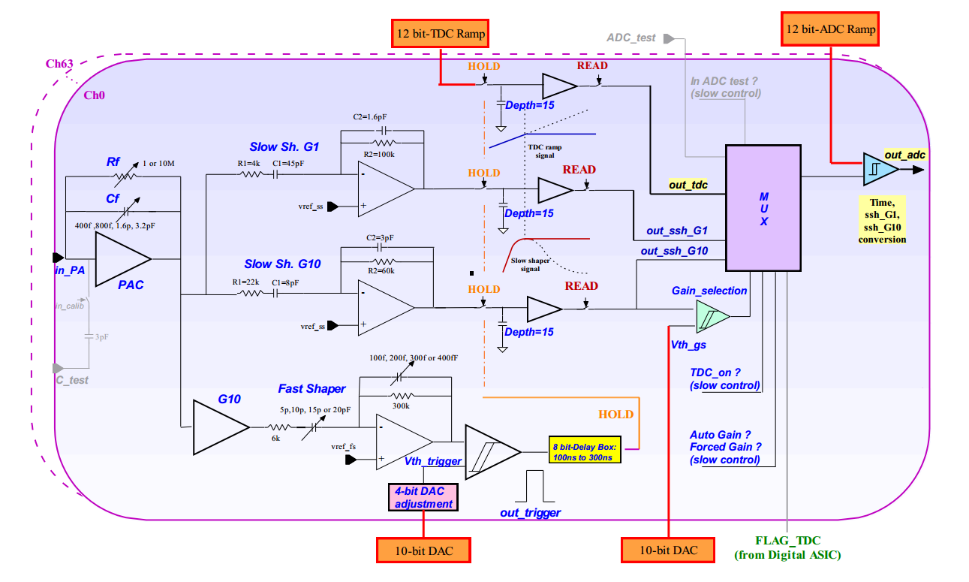


Fig. 2 The schematic illustration of the analog part of SKIROC2 (one channel).

The input signal passes through the CSA with the variable gain set by switchable Feedback Capacitance (Cf) array. And the output of CSA is fed to the fast and slow shapers for trigger and precise measurement. By comparing fast shaper’s output with a threshold set by an 10 bit on-chip Digital-to-Analog Convertor (DAC), the discriminator generates a trigger signal to hold the voltages at two slow shaper outputs, which are optimized for low-noise charge measurement, on the SCAs. The signals on the SCAs are read out and converted by a 12-bit Wilkinson ADC, with a bunch ID tagged on a 10 MHz clock, then saved in the on-chip memory.

Benefited from the two different-gain slow shapers and the adjustable-gain CSA, the SKIROC2 has a wide dynamic range, ensuring a linear response for equivalent input charge up to +3000 fC, with a noise of as low as 0.2 fC. The peak time of the chip is tuneable from 50 ns to 200 ns to suit different signals and the power consumption is about only 6 mW per channel. In addition, the SKIROC2 can be configured to be either self-triggered or ex-triggered, and this satisfies different experiment conditions. Since these features meet the requirements of the Si-PIN diode, the SKIROC2, as a result, is chosen as the readout chip of the system.

## Front-end Board

The FEB, which accommodates one SKIROC2 chip and 64 detectors, is divided into two parts: the Detector-Part and the ASIC-Part, so that it is convenient to test different kinds of Si-PIN diodes without redesigning the ASIC-Part. The ASIC-part is mainly designed to make the SKIROC2 functions well. Besides, there are three ERNI-154744 connectors adopted on the ASIC- Part, two of which are responsible for communication with the DIF6, and the other one is for gathering detectors’ outputs from Detector-Part. The control signals as well as output data of SKIROC2 go through the two connectors connecting with the DIF.

In addition, there are two kinds of control signals, depending on the speed: the fast control and the slow control. The fast control, which is in charge of SKIROC2’s clock, trigger and reset or validate the SCA, connects to the control center of SKIROC2 directly through Low Voltage Differential Signal pairs (LVDS). And the slow control is, on the other hand, in a daisy chain cascade and configures the 616-bit registers on the chip, which store some configurations such as the feedback capacitance of the CSA and the trigger mode. The digitalized output data of the SKIROC2 are sent to the DIF through the Open Collector (OC) gate. Considering the OC gate and the daisy chain cascade, it is very convenient to expand the FEB for more ASICs without changing the definition of the connector to DIF.



Fig. 3 Block diagram of Front-end Board, which consists of Detector part and ASIC part.

The Detector-Part carries a Si-PIN diodes array and supplies them. At present, a kind of Si-PIN diodes named S5980 from HAMAMATSU is taken to test the performance of the system7. The active area of the diode is 5 × 5 mm2 and the thickness of depletion layer is 80µm, leading to a result of low reverse voltage demand (about 10 V). And the other advantages of the diode are that the dark current is only 100 pA and the thermal capacitance of detector is as small as 10 pF. Since the output noise of the diode is sensitive to the High Voltage (HV) ripple, the cathode of the diode is connected to a HV of 13 V, supported by a well-designed Low-DropOut regulator (LDO, TPS7A4700 from Texax Instruments company) with the high power supply ripple rejection of 82 dB. The anode of the diode is directly connected to SKIROC2’s input, which supplies a reference voltage about 1 V to ensure the correct working status of the Si-PIN diode.

## Data Interface

The DIF consists of four main parts: the FPGA part, the connector part, the power supply part and the interface part. The FPGA part is mainly composed of an FPGA (ARTIX7, Xilinx) and a PROM (N25Q128). The function of the FPGA is to implement the required logic to control the FEB and to communicate with the PC. The connector part to FEB is via two ERNI-154744 connectors, as mentioned before. The supply part is implemented with a DC input (5V) from outside and several LDO regulators, generating supply for the DIF and the FEB. The interface part is in charge of communicating with PC through a mini-USB port, realized by a USB chip CY7C68013. In addition, an optical transceiver interface is remained for compatibility with other readout device.



Fig. 4 Block diagram of logic implemented in the FPGA

The logic diagram of the FPGA is presented in Fig. 4. The acquisition module controls the ASIC to work in normal mode and process the data from SKIROC2, which are first stored in the FIFO, then packed and finally transferred to PC. The trigger module is in charge of generating a trigger when the external trigger is in need, while normally the chip is self-triggered. The calibration module and S-curve module are used to control the ASIC during calibration or testing, which is elaborated below. The optical module and USB module are responsible for receiving commands and transmitting data to the server.

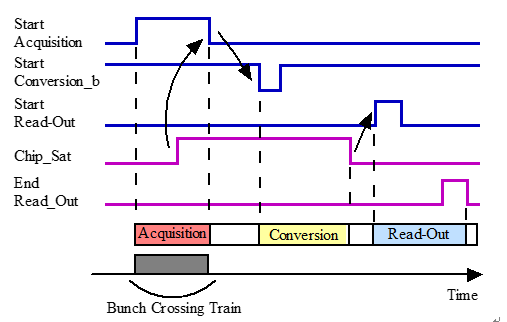


Fig. 5 Global timing control of data acquisition for SKIROC2

The timing control sequence of the main signals during the normal acquisition progress is shown in Fig. 5. This global sequencing is made around three signals from FPGA on the DIF: StartAcquisition, StartConversionb and StartReadout. In response to the three signals, the SKIROC2 answers with two signals: Chip\_Sat and End\_Readout. The acquisition is composed of 3 phases: Acquisition, Convertion and Readout. The acquisition phase starts when the StartAcquisition has a rising edge and ends when this signal falls. During the acquisition phase, the SKIROC2 outputs a rising edge of Chip\_Sat signal, informing that the 15-depth SCA array is full. By giving a falling edge of StartConvsionb, the SKIROC2 begins to convert signals from analog to digital. When the conversion is finished, the Chip\_Sat signal falls and a rising of StartReadout signal is sent from DIF to SKIROC2, starting the readout phase. The End\_Readout rises when the transmission is over. It is worth noting that the End\_Readout signal is in daisy chain that the following SKIROC2’s readout phase could be started by this signal, if there are more than one ASIC.

The prototype electronics system has been implemented and the picture of the FEB and the DIF is shown in Fig. 6.



Fig. 6 The photograph of FEB and DIF.

# Characterization

We have carried out a number of characterizations to assess the performance of the system. The results of basic output, baseline noise and calibration of SKIROC2, trigger efficiency, X-ray test and cosmic test are presented and discussed below.

## Basic output of SKIROC2

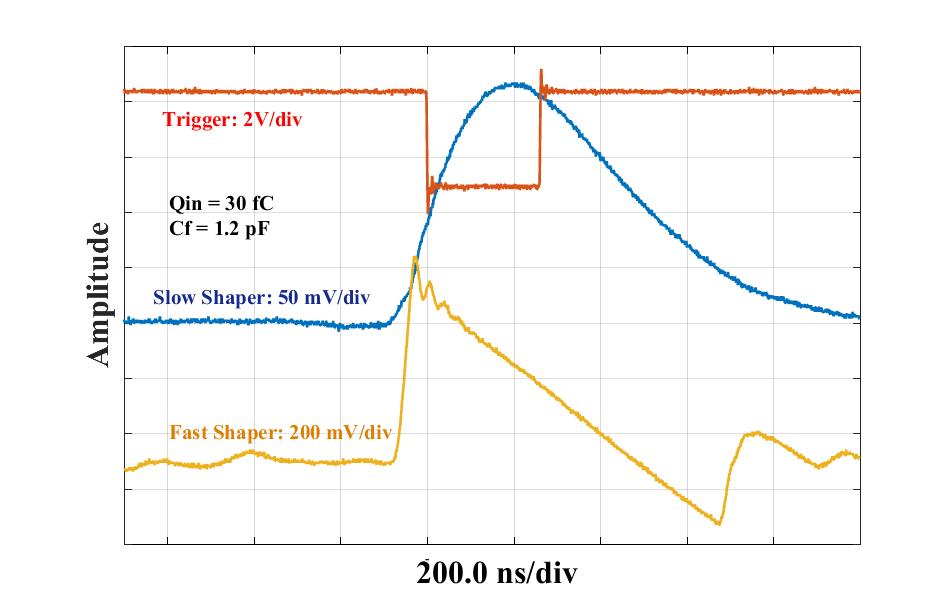


Fig. 7 The typical outputs of the fast shaper, slow shaper and trigger from single channel.

Although the SKIROC2 is designed to send out digitalized data, an analog probe is remained to observe the outputs of analog part for debugging. The basic outputs, such as slow shaper, fast shaper and trigger, of every channel was observed to make sure that all channels were in correct status. A typical waveform of the fast shaper, slow shaper and trigger from single channel is shown in Fig. 7. From the waveform, the fast shaper is about 200 ns ahead of the peaking time, so that a trigger from the discriminator next to the fast shaper could be used to hold the peak of the slow shaper output.

## Baseline and noise

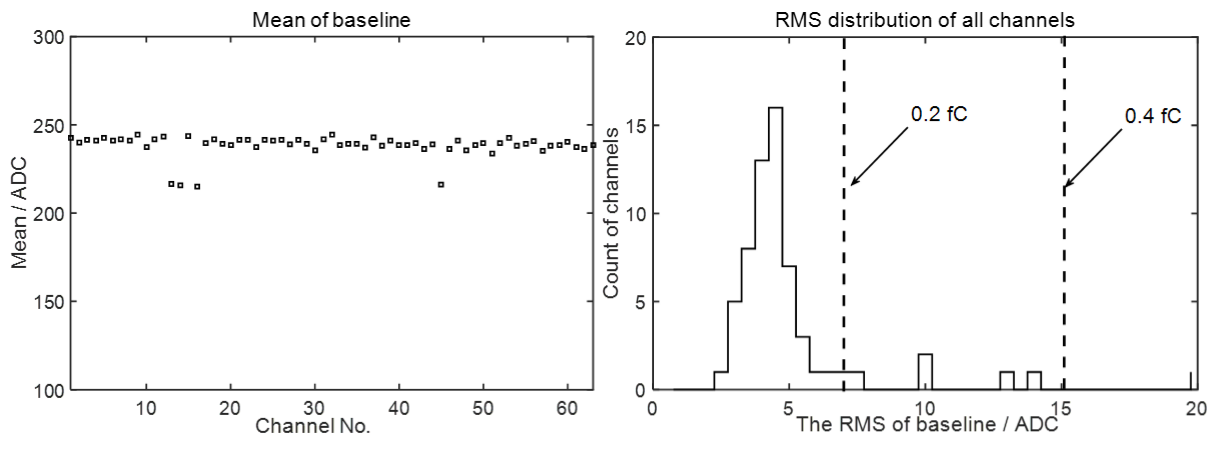


Fig. 8 The baseline and noise distribution of all 64 channels.

In order to evaluate the noise level of the system, the external trigger function of SKIROC2 was used to get the pedestal of the system without detectors. Since the SKIROC2 requires 4 ms for conversion phase and readout phase, triggers in a fixed time interval of 10 ms were generated by the DIF, controlling the acquisition of the baseline. The chip held the baselines of all 64 channels and converted them to digital when triggered. Fig. 8 shows the average of baselines and sigma of noise from all channels. The results showed that not all channels exhibited excellent baseline and noise results, but most channels demonstrated a noise level lower than 0.2 fC equivalent input charge. The noise level meets the requirements of the Si-PIN diode, considering that the maximum was less than 0.4 fC.

## Calibration

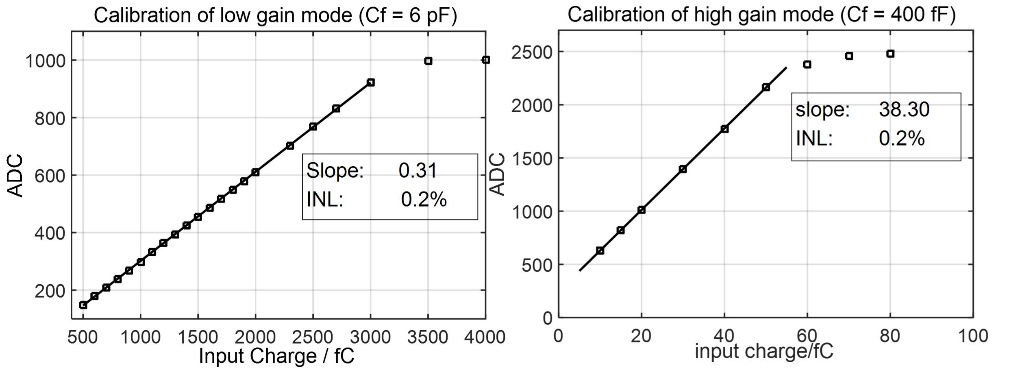


Fig. 9 The linear fit results of two gain modes of SKIROC2.

The calibration assessment was carried out to obtain the linearity and dynamic range of the SKIROC2 chip. By taking advantage of the SKIROC2’s 3 pF calibration capacitors on each channel, the self-calibration was conducted by the procedure elaborated below. A waveform generator with attenuator was used to generate step pulses with different amplitudes. When the step pulses were applied to the on-chip capacitor, a certain amount of charge, which covered the full range, was injected into every channel of SKIROC2 from the test pulse input for performance assessment. The SKIROC2 chip has many operation modes by tuning the Cf array. The measurement was carried out with the highest gain mode (Cf = 400 fF) and lowest gain mode (Cf = 6 pF). The gain uniformity between different channels was better than 5% and the typical linear curves of output ADC code versus input charge, of the two modes, are shown in Fig. 9. Fig. 9 shows that the linear range of the highest gain mode and the lowest gain mode were 50 fC and 3 pC, respectively. The Integral non-linearities (INL) of both modes reached up to 0.2%.

## Trigger efficiency



Fig. 10 The trigger efficiency for two channels as a function of threshold setting for an input charge of 2 fC.

The trigger efficiency was obtained from an “S-curve” as presented in Fig. 10. The trigger threshold was set by two digital-to-analog conversion (DAC) settings on chip: a global threshold with a 10-bit DAC and channel by channel adjustment with a 4-bit DAC. To measure the trigger efficiency, a fixed amount of charge was introduced from the test pulse input. If the fast shaper pulse exceeds the threshold, the SKIROC2 chip generates a trigger signal for counting. The S-curve was obtained by varying the trigger threshold 10-bit DAC and recording the efficiency at each DAC code. The curve was fitted by a complementary error function, the centre value corresponds to the charge threshold and the sigma parameter represents the noise-induced width. The results of the curve is closed to the previous work finished by T. Suehara8. The 4-bit DAC adjustment for every channel should help to get a better threshold uniformity, but this function did not work properly in SKIROC2 due to a detected bug, which has been fixed in a newer version of SKIROC2a.

## X-ray test and Cosmic ray test



Fig. 11 The spectrum of the X-ray of 241Am (left) and the pedestal and MIP distribution of cosmic ray (right).

Several Si-PIN diodes of S5980 were coupled with the system to test the performance. A joint test with an X-ray source of 241Am and a test with cosmic ray were carried out. During both the tests, the output of diodes were directly sent to the SKIROC2, which was set to work in the highest gain mode. The spectrum of 59 keV X-ray is shown in the left one of the Fig. 11. It can be observed that the shape is not a standard Gaussian, which is because there is a certain chance that the photon has photoelectric effect before the depletion layer and losses some energy. According to the calibration results, the equivalent input charge was 2.89 fC and the resolution was 13.3% (in RMS). The right one of the Fig. 11 is the result of cosmic ray test from a single channel. The SKIROC2’s trigger threshold was set at 0.5 Minimum Ionizing Particle (MIP, with about 5 σ separation of the noise) to get signal from cosmic ray. In addition, there was a random external trigger to get the pedestal noise. The spectrum of the cosmic ray was Landau fitted and the pedestal was Gaussian fitted. The results of the fits showed that the Signal-to-Noise Ratio (SNR) for MIP was 10.9, which was closed to the test results of other electronics using SKIROC2 ASIC9. These tests show that the system has enough resolution to identify small signals such as X-ray and MIP.

# Conclusions

In this paper, a SKIROC2-based prototype electronics system for Si-PIN array, as well as the performance test, have been presented. The system, which consists of FEB module and DIF module, has features of high integration, low noise and high dynamic range, which are suitable for Si-PIN array. Considering the daisy chain structure of the SKIROC2, it is easy to expand the FEB for more ASICs without changing the interface protocol. The SKIROC2, as well as the design concept of the electronics system could be a preliminary study on the prototype of Si-W ECAL for CEPC.

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